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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,765	11/07/2001	Franck Roche	00RO30454288	9186

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EXAMINER	
PATEL, NIMESH G	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 05/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,765	ROCHE ET AL.	
	Examiner	Art Unit	
	Nimesh G. Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *20-52* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *20-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 20-52 are rejected under 35 U.S.C. 102(b) as being anticipated by the I2C-Bus Specification, hereinafter referred to as I2C.

3. Regarding claim 20, I2C discloses a method of transmitting data between two devices via a clock line(Figure 2, SCL) and at least one data line(Figure 2, SDA), the clock line being maintained by default on a first logic value(Page 8, Section 5; HIGH), the method comprising: providing each device with the ability to tie the clock line to a potential representing a second logic value(Page 8, Section 5; LOW) opposite the first logic value; tying the clock line to the second logic value, via the two devices, when data is transmitted(Page 9, Section 6.2); maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent(Page 10, Section 7.1; Page 13, Section 8.3).

4. Regarding claim 21, I2C discloses a method wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted(Page 9, Section 6.2).

5. Regarding claim 22, I2C discloses a method wherein the master device ties the clock line to the second logic value after applying data to the data line when the master device is sending the data to the slave device(Figure 5).

6. Regarding claim 23, I2C discloses a method wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(Figure 5).

7. Regarding claim 24, I2C discloses a method wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Page 10, Section 7.1).

8. Regarding claim 25, I2C discloses a method wherein the master device ties the clock line to the second logic value when the master receives data from the slave device(Figure 5).

9. Regarding claim 26, I2C discloses a method wherein the slave device detects the second logic value on the clock line then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device(Page 7, Section 4).

10. Regarding claim 27, I2C discloses a method wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line(Page 10, Section 7.1).

11. Regarding claim 28, I2C discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 5).

12. Regarding claim 29, I2C discloses a method further comprising providing the slave device with a communication interface circuit including: trigger means for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value(Page 10, Section 7.1); an input for applying a clock line release signal to the trigger means; and an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger means and a second value when the clock line is released by the trigger means(Page 10, Section 7.2).

13. Regarding claim 30, I2C discloses a method, wherein the communication interface circuit further comprises: means for storing at least one data; and means for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value(Figure 3).

14. Regarding claim 31, I2C discloses a method, wherein the first logic value is 1 and the second logic value is 0(Figure 5).

15. Regarding claim 32, I2C discloses a method of transmitting data between two devices connected via a clock line(Figure 2, SCL) and at least one data line(Figure 2, SDA), the method comprising: maintaining the clock line on a first logic value as a default(Page 8, Section 5; HIGH); providing each device with the ability to tie the clock line to a potential representing a second logic value(Page 8, Section 5; LOW); tying the clock line to the second logic value, via the two devices, when data is transmitted(Page 9, Section 6.2); maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and maintaining the data on the data line by the device sending the data at least until the clock line is released by the device to which the data is sent(Page 10, Section 7.1; Page 13, Section 8.3).

16. Regarding claim 33, I2C discloses a method, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic

value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted(Page 9, Section 6.2).

17. Regarding claim 34, I2C discloses a method, wherein the master device ties the clock line to the second logic value after applying data the data line when the master device is sending the data to the slave device(Figure 5).

18. Regarding claim 35, I2C discloses a method, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value and reads the data, when the slave device is receiving the data from the master device(Figure 5).

19. Regarding claim 36, I2C discloses a method, wherein a time period that the slave device has to release the clock line after receiving data, is independent of any action by the master device, as the master device does not send any new data while the slave device has not released the clock line(Page 10, Section 7.1).

20. Regarding claim 37, I2C discloses a method, wherein the master device ties the clock line to the second logic value when the master receives data from the slave device(Figure 5).

21. Regarding claim 38, I2C discloses a method, wherein the slave device detects the second logic value on the clock line, then ties the clock line to the second logic value, and applies the data to the data line, when the slave device is sending data to the master device(Page 7, Section 4).

22. Regarding claim 39, I2C discloses a method wherein a time period that the slave device has to release the clock line after sending the data, is independent of any action by the master device, as the master device does not tie the clock line to the second logic value to request a new data until the slave device has released the clock line(Page 10, Section 7.1).

23. Regarding claim 40, I2C discloses a method wherein when the clock line has the first logic value, a time period that the master device has to tie the clock line to the second logic value is independent of any action by the slave device(Figure 5).

24. Regarding claim 41, I2C discloses a method providing the slave device with further a communication comprising interface circuit including: a trigger circuit for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value(Page 10, Section 7.1); an input for applying a clock line release signal the trigger circuit; and an output for delivering a status signal that has a first value when the clock line is tied to the second logic value by the trigger circuit and a second value when the clock line is released by the trigger circuit(Page 10, Section 7.2).

25. Regarding claim 42, I2C discloses a method wherein the communication interface circuit further comprises: a buffer for storing at least one data; and a circuit for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value(Figure 3).

26. Regarding claim 43, I2C discloses a method wherein the first logic value is 1 and the second logic value is 0(Figure 5).

27. Regarding claim 44, I2C discloses a data transmitting/receiving device comprising: a clock line connection terminal for connection to a clock line(Figure 2, SCL); at least one data line connection terminal for connection to a data line(Figure 2, SDA); means for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high); and data sending means for waiting for the clock line to have the first logic value(Page 10, Section 7.1), applying data to the data line, tying the clock line to the second logic value, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent(Figure 6).

28. Regarding claim 45, I2C discloses a device, further comprising data receiving means for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading data on the data line, then releasing the clock line, when the data is to be received(Figure 6).

29. Regarding claim 46, I2C discloses a data transmitting/receiving device comprising: a clock line connection terminal for connection to a clock line(Figure 2, SCL); at least one data line connection terminal for connection to a data line(Figure 2, SDA); means for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 10, Section 7.1); and means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading data on the data line, and releasing the clock line, when the data is to be received(Figure 6).

30. Regarding claim 47, I2C discloses a device, further comprising means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line the second logic value, applying data to the data line, and releasing the clock line, when the data is to be sent(Page 7, Section 4).

31. Regarding claim 48, I2C discloses a synchronous data transmission system comprising: a clock line(Figure 2, SCL); a data line(Figure 2, SDA); a master data transmitting/receiving device(Figure 2, Microcontroller A) comprising a clock line connection terminal connected to the clock line, at least one data line connection terminal connected to the data line, means for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high)(Page 10, Section 7.1), and data sending means for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, data is to be sent(Figure 6); and a slave data

transmitting/receiving(Figure 2, Microcontroller B) comprising a clock line connection terminal connected to the clock line; at least one data line connection terminal connected to the data line; means for tying the clock line to the potential representing the second logic value(low); and means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line to the second logic value, reading the data on the data line, and releasing the clock line, when the data is to be received(Figure 6).

32. Regarding claim 49, I2C discloses a system, wherein the master device further comprises data receiving means for waiting for the clock line to have the first logic value, tying the clock line to the second logic value, reading the data on the data line, then releasing the clock line, when the data is to be received by the master device(Page 7, Section 4).

33. Regarding claim 50, I2C discloses a system, wherein the slave device further comprises means for detecting a change from the first logic value to the second logic value on the clock line, tying the clock line the second logic value, applying the data to the data line, and releasing the clock line, when the data is to be sent from the slave device(Page 7, Section 4).

34. Regarding claim 51, I2C discloses a communication interface circuit for connection to a data transmitting/receiving device via a clock line(Figure 2, SCL) and at least one data line(Figure 2, SDA), the circuit comprising: means for tying the clock line to a potential representing a second logic value(low) that is the opposite of a first logic value(high); trigger means for automatically tying the clock line to the second logic value when the clock line is changing from the first logic value to the second logic value(Page 10, Section 7.1); an input to apply a clock line release signal to the trigger means; and an output to deliver an information signal that has a first value when the clock line is tied to the second logic signal by the trigger means and a second value when the clock line is released by the trigger means(Page 10, Section 7.2).

35. Regarding claim 51, I2C discloses a communication interface circuit further comprising: means for storing data; and means for automatically applying the data to the data line when the clock line changes from the first logic value to the second logic value(Figure 3).

Response to Arguments

36. Applicant's arguments filed February 21, 2006 have been fully considered but they are not persuasive. Applicant argues that I2C does not teach or fairly suggest that the master and slave devices each has the ability to tie the clock line to a potential representing a second logic value different than a first logic value and then tying the clock line to a potential representing a second logic value, via the two devices, when data is transmitted. Examiner respectfully disagrees. I2C discloses master and slave devices each having the ability to tie the clock line to a potential representing a second logic value different than a first logic value and then tying the clock line a potential representing a second logic value(Page 8, Section 5; LOW) opposite the first logic value; tying the clock line to the second logic value, via the two devices, when data is transmitted(Page 9, Section 6.2; Page 10, Section 7.1; Page 13, Section 8.3). The default logic for the clock is HIGH. The master device controls the clock and therefore has the ability to tie the clock to a LOW level. The slave device can stretch the clock by holding down the clock to a LOW level. Therefore both the master and slave devices can tie the clock to a LOW level(Page 13, Section 8.3).

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G. Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

REHANA PERVEEN
SUPERVISORY PATENT EXAMINER
5/10/06

NP
May 9, 2006